HPC@Intel: On Driving Industrial Innovation

Dr. Stephen Wheat
General Manager, HPC
Intel Corp.

Agenda

To Compete You Must Compute

Neo-heterogeneity: The Future of Technical Computing Hardware

The Imperative: Modernizing Code

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Neo-heterogeneity: The Future of Technical Computing Hardware

The Imperative: Modernizing Code

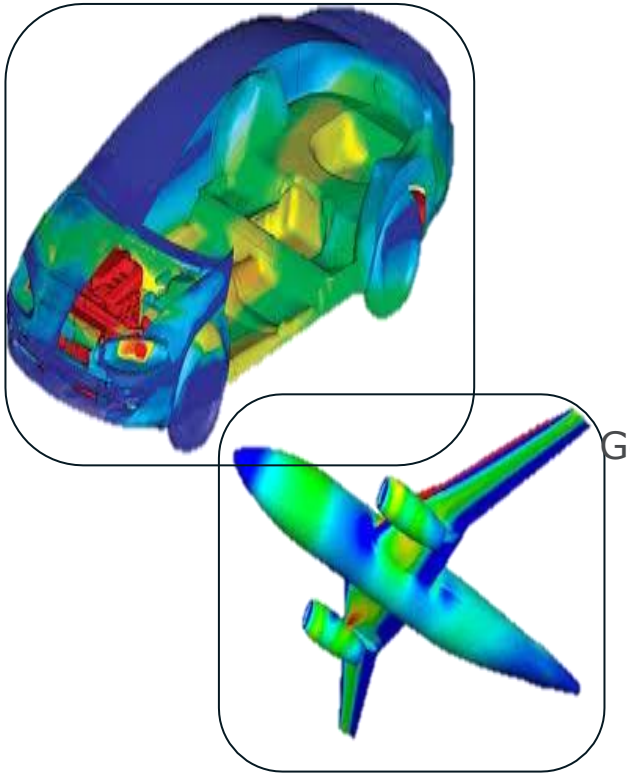
Dated, but still very relevant story to explain HPC

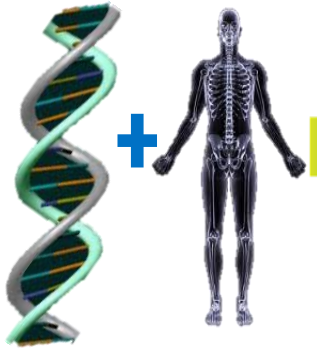
Why HPC in multimedia form

Technical Computing Continues Its Rapid Growth

To Compete, You Must Compute

Governments & Research | *Commercial/Industrial* | *New Users – New Uses*





Genomics Clinical Information

From Diagnosis to personalized treatments quickly

Source: IDC: Worldwide Technical Computing Server 2013–2017 Forecast; Other brands, names, and images are the property of their respective owners.

Dyson Creates a Revolutionary Fan

Utilizing new scientific method

Reduced the number of costly, time-consuming physical prototypes

2.5x better fan performance while eliminating external moving parts

By investigating 10x the number of design possibilities using virtual prototyping

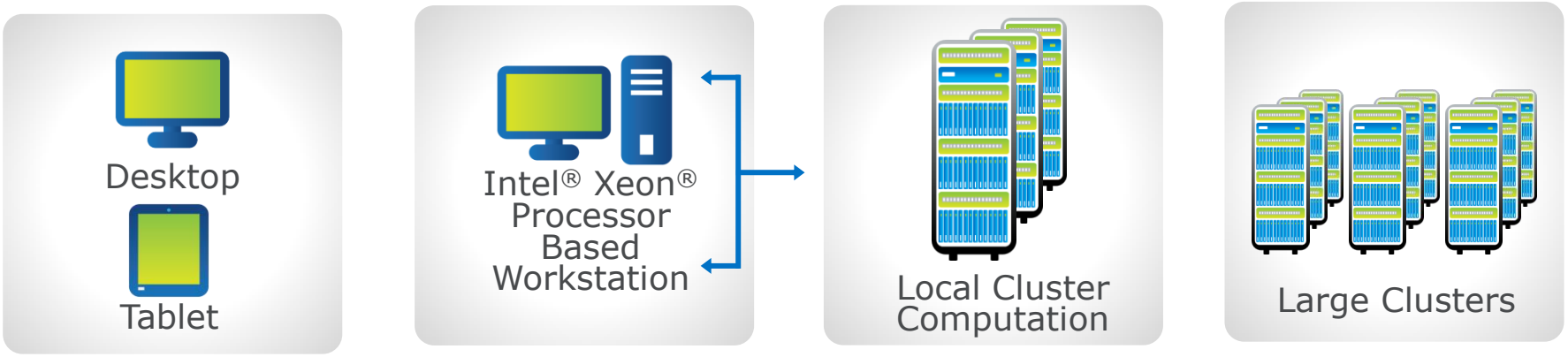
Virtual prototype

Dyson Air Multiplier Fan

Source: Ansys Advantage Volume IV, Issue 2 2010 pp. 5-7

The Right Tool for the Job: A Continuum of Computing

How do you get breakthroughs for your investment



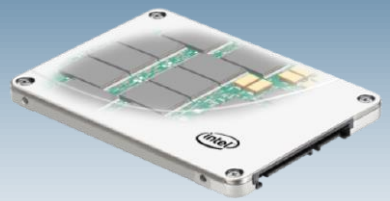
Common underlying architecture scales investments across technical computing platforms

Building the Right Tool for the Job

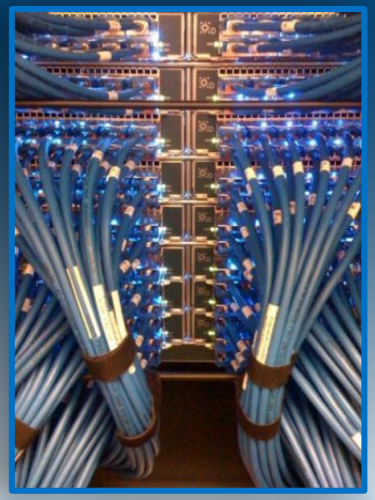
Balanced compute, storage, and interconnects based on workload

COMPUTE

STORAGE



NETWORKING



SOFTWARE

Audi Workflow

Real-time, photo-realistic predictive rendering

Topline Innovation

More compelling, accurate visualization of car design

Avoid physical prototyping spin by identifying body part fit issues

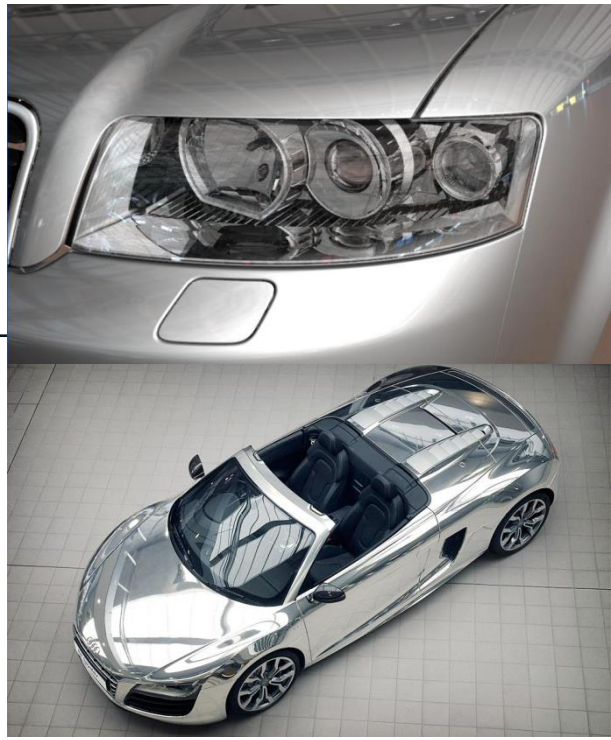
Reduce turn-around from identifying design changes

Bottom-line Costs

Get the most for their Autodesk software investment with optimized performance on Intel platforms

Intel® Xeon® Processor E5-2600 product family based solution across workstations and clusters reduced deployment and maintenance costs

Audi Truth In Engineering



Virtual prototyped images

Images courtesy of The Audi Group, Used by permission

Audi Results

Better, safer cars to market quicker

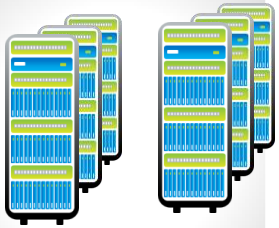
Audi
Truth In Engineering

Intel® Xeon ® Workstation

Upgraded 2000 workstations to latest Intel® Xeon® processor E5-2600 product family

Local Cluster Computation

Phase 1: 450 dual-processor nodes. Phases 2 & 3 will duplicate 1,350 node visualization cluster



Large Cluster

Scaled Autodesk Opticore V13 on 1024 Intel® Xeon® processor E5-2600 product family

Result: Reduced physical prototypes

Images courtesy of The Audi Group, Used by permission

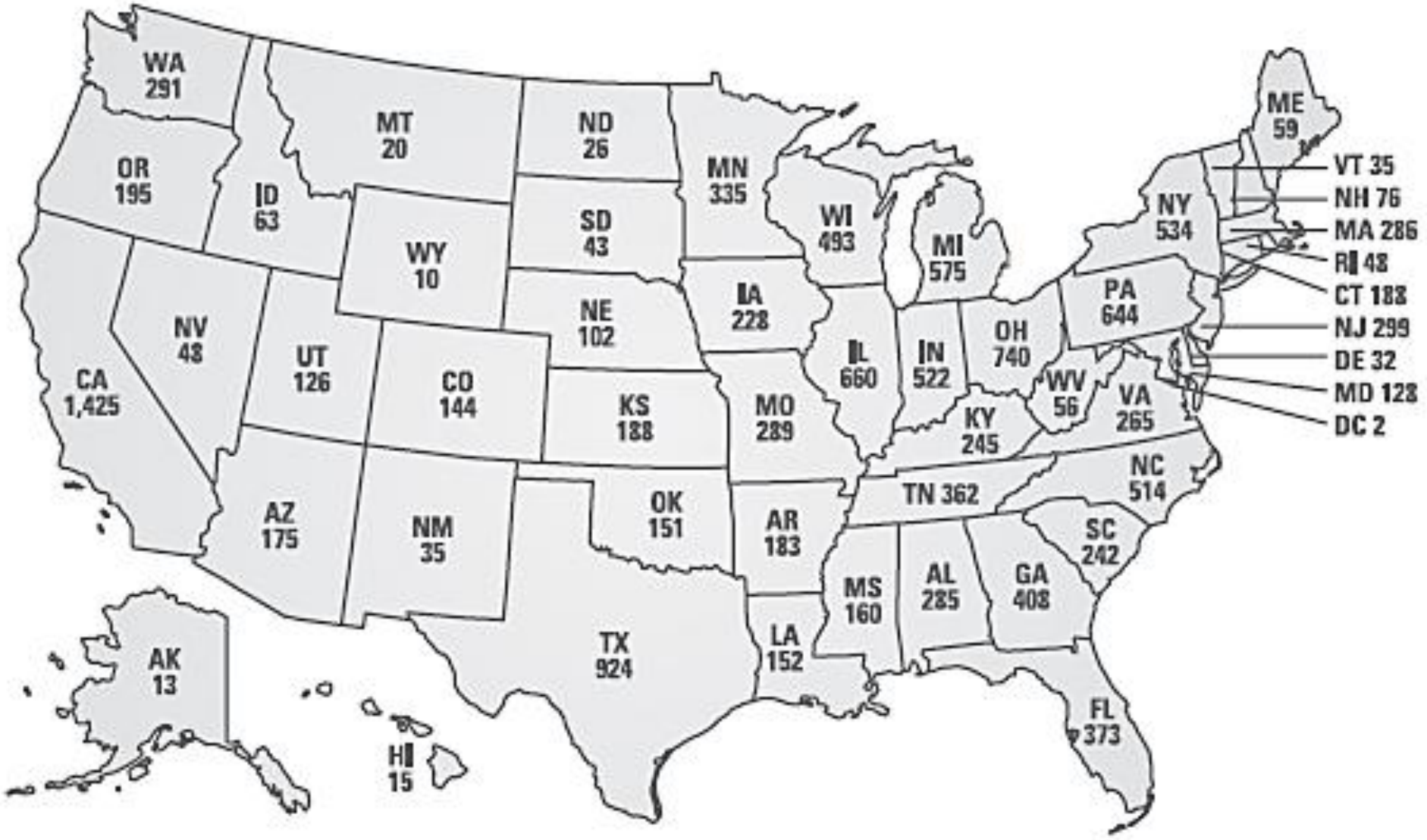
It’s not just the Tier 1 OEMs

On the Missing Middle in Manufacturing

International update

Local update

Manufacturing Jobs in the USA (K)



Source: U.S. Bureau of Labor Statistics, 2008

And it’s not just reaching the SMMs

An update on the Wheeling program

Making A New Reality Faster Than Ever

From Vision to Reality: Without Prototypes!

Audi
Truth in Engineering

2000 2005 2010 2013

Goal: Increase level of detail & reality and opportunity to experience a product before it is built

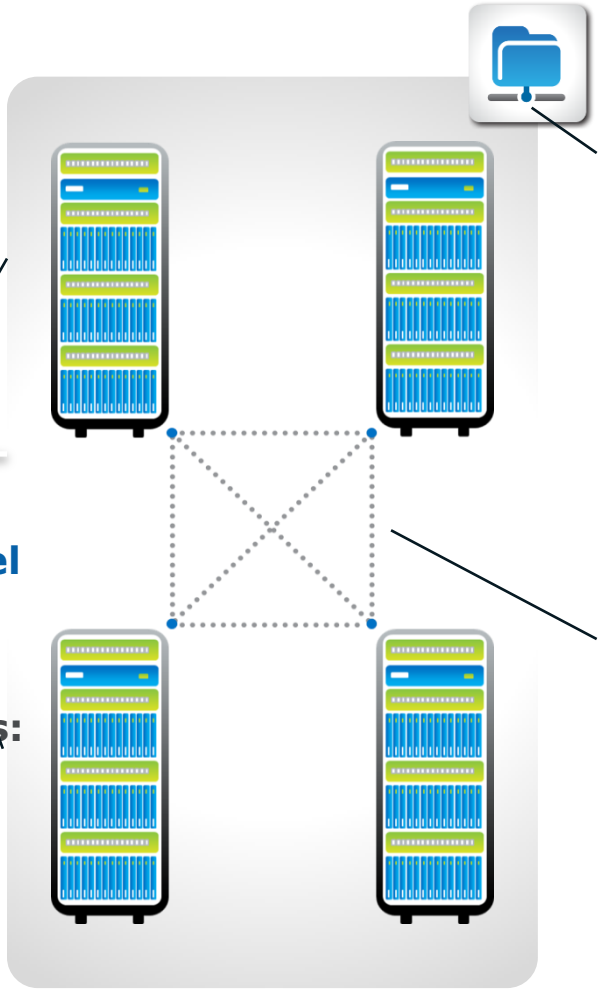
Goal: Reduction of physical cars needed for decision process > cost reduction, process speed up

"**For Audi to stay on the forefront of automotive design**, *we required a new way to visualize our designs. Working with Intel and Autodesk, we have been able,* **for the first time**, *to adopt* **Real Time Predictive Rendering** *to interactively see our car design concepts with high fidelity visualization. This helps us reduce the costs of development by* **eliminating expensive prototype turns**" -- **Audi**

What Makes a Great HPC Cluster?

Industry-leading workload performance

Intel® Xeon® processors:



Fast, reliable access to data

Intel Xeon processor based storage

Intel® SSDs

Intel® Enterprise Edition for Lustre* software

Performance for highly-parallel workloads while preserving software investment

Intel® Xeon Phi™ coprocessors:

Fast, cost-effective data movement between nodes

Intel® True Scale fabric

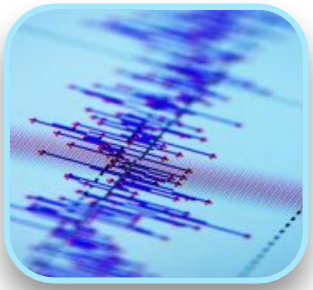
Ease of deployment and maintenance

Intel® Cluster Ready

Intel: The Architecture for Discovery

Intel® Xeon® Processor E5-2600 V2 Family

Expect average increase of 1.3x across real-world applications

CAD/CAE	Energy	Life Sciences	Finance
			
UP TO 1.37x	UP TO 1.59x	UP TO 1.38x	UP TO 1.32x

CAD/CAE Configuration (Ansys Fluent v14.0*):
2S IVB Romley-EP: E5-2697 v2 (2.7GHz CPU X 2 w/ 12 Cores), 64G Mem; OS: RHEL 6.4
2S SNB Romley-EP: E5-2690 (2.9GHz CPU X 2 w/ 8 Cores), 64G Mem; OS: RHEL 6.3

Energy Configuration (Paradigm® GeoDepth® v2011.3):
2S IVB Romley-EP: E5-2697 (2.7GHz CPU X 2 w/ 12 Cores), 64G 1867 Mem; OS: RHEL 6.4
2S SNB Romley-EP: E5-2670 (2.6GHz CPU X 2 w/ 8 Cores), 64G 1600 Mem; OS: RHEL 6.3

Life Sciences Configuration (PerkinElmer Acapella* v3.1.0):
2S IVB Romley-EP: 2.7GHz CPU X 2 w/ 12 Cores, 32G 1867 Mem; OS: Windows Server 2008 R2 with SP1 (x64)
2S SNB Romley-EP: 2.7GHz CPU X 2 w/ 8 Cores, 32G 1600 Mem; OS: Windows Server 2008 R2 with SP1 (x64)

Finance Configuration (SunGard Adaptiv* Benchmark X 13.1):
2S IVB Romley-EP: E5-2697 v2 (2.7GHz CPU X 2 w/ 12 Cores), 64G Mem; OS: Win Server 2008 R2
2S SNB Romley-EP: E5-2680 (2.7GHz CPU X 2 w/ 8 Cores), 64G Mem; OS: Win Server 2008 R2

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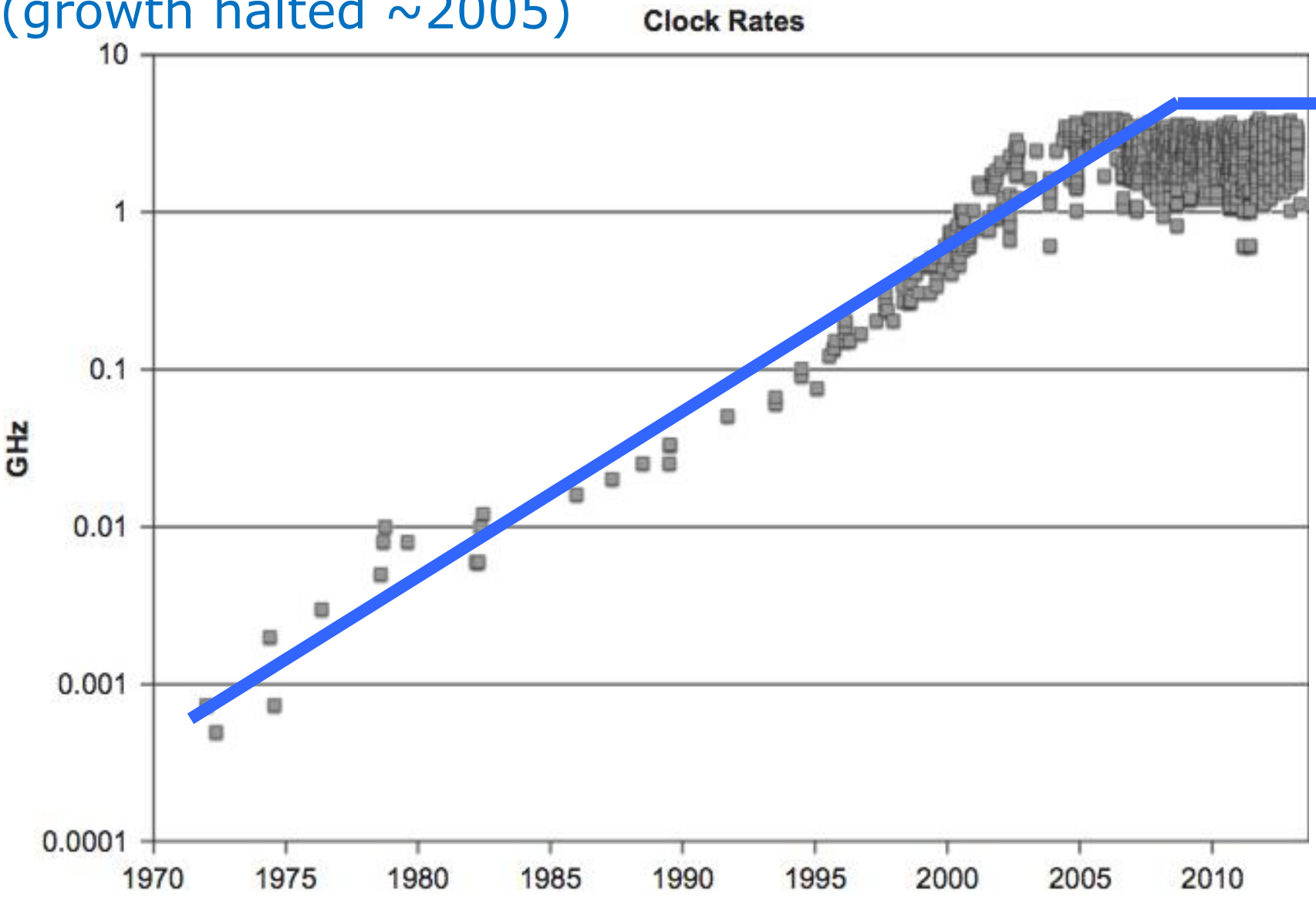
The Imperative: Modernizing Code

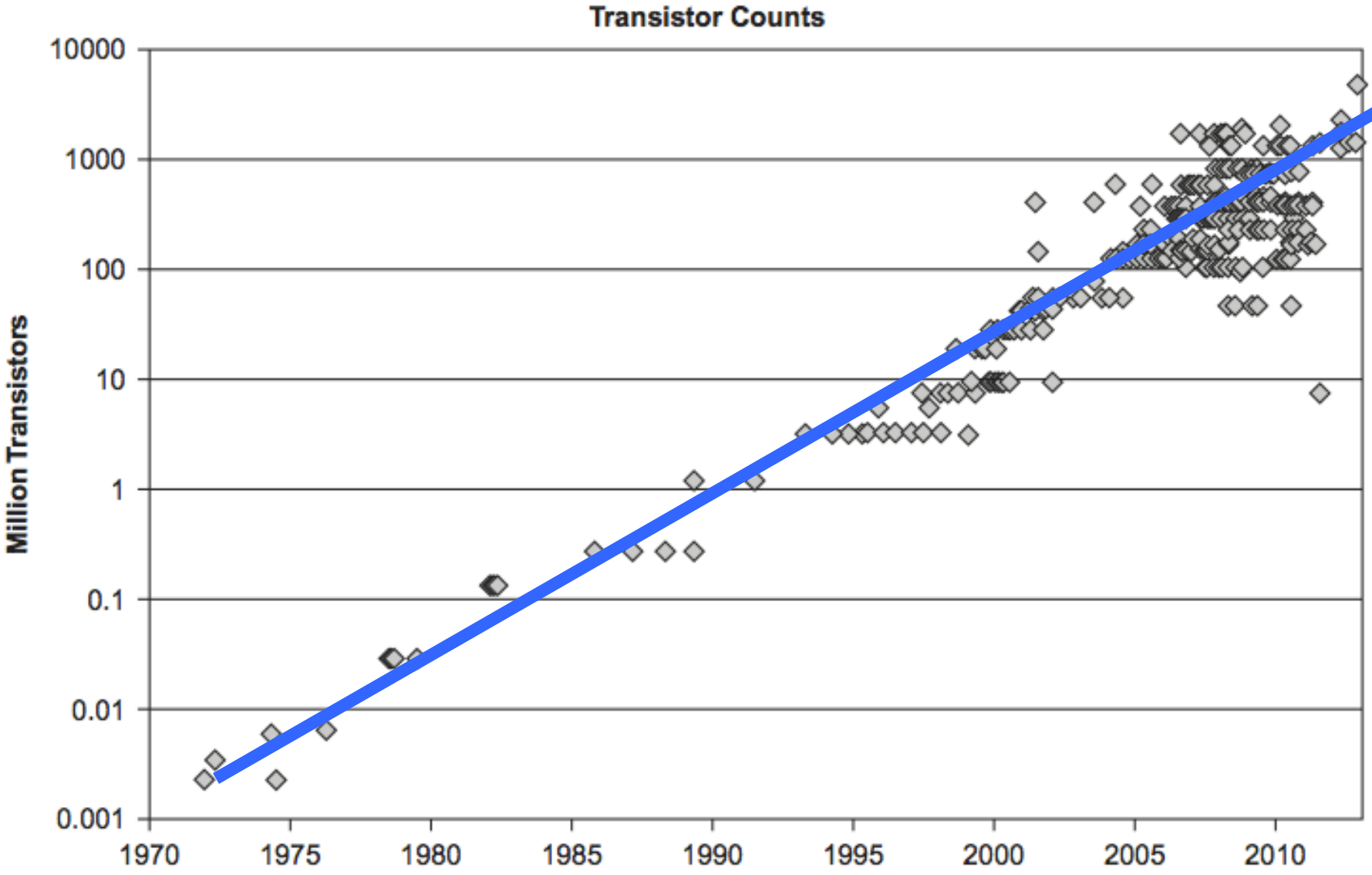
Wrap up

Processor Clock Rate (growth halted ~2005)



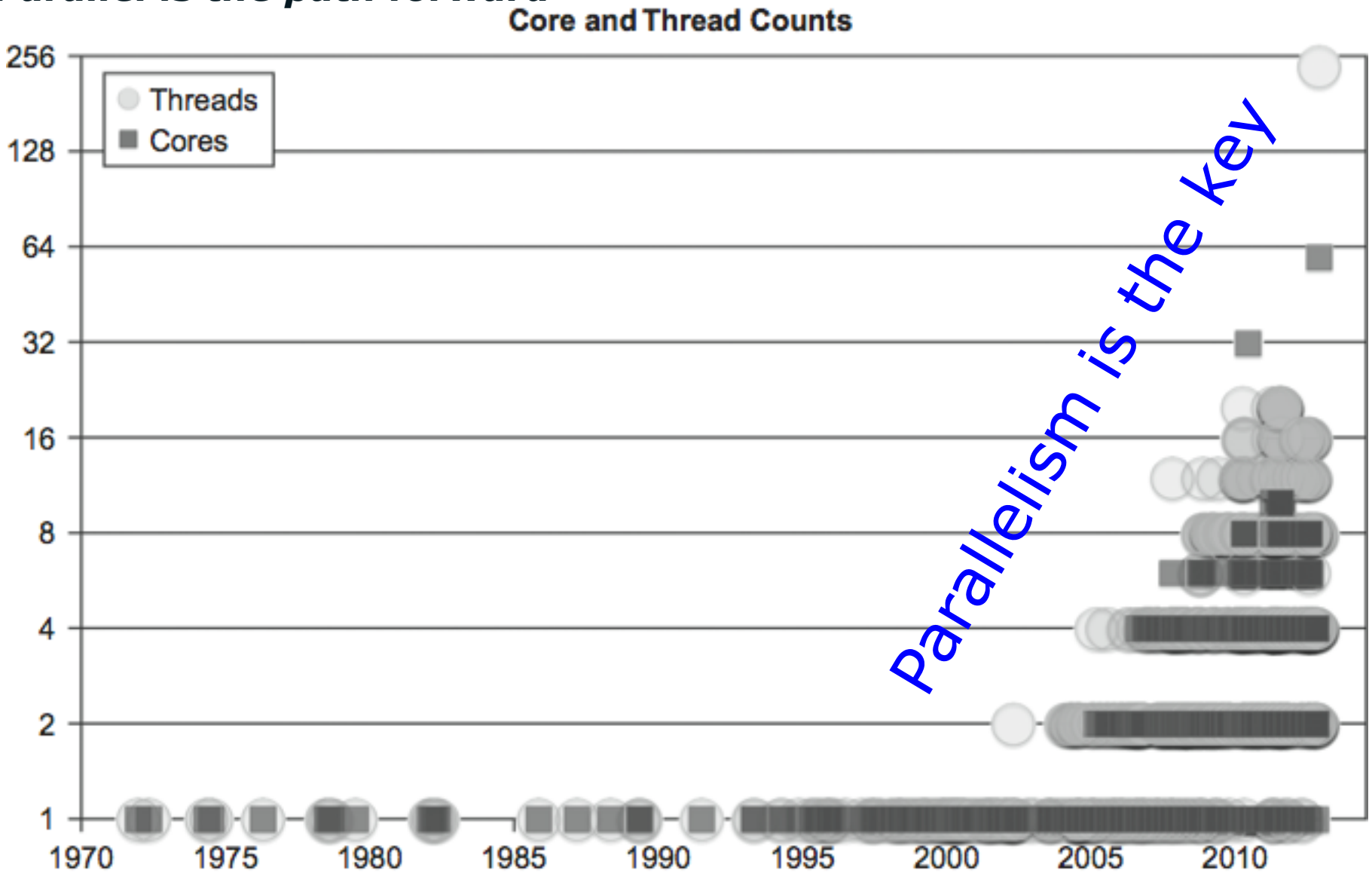
Transistors per Processor

Continuing to grow (Moore's Law)



Thread and Core Count Growth

Parallel is the path forward



Two Types of Parallelism for Programmers to Identify and Use

Scaling (more cores)

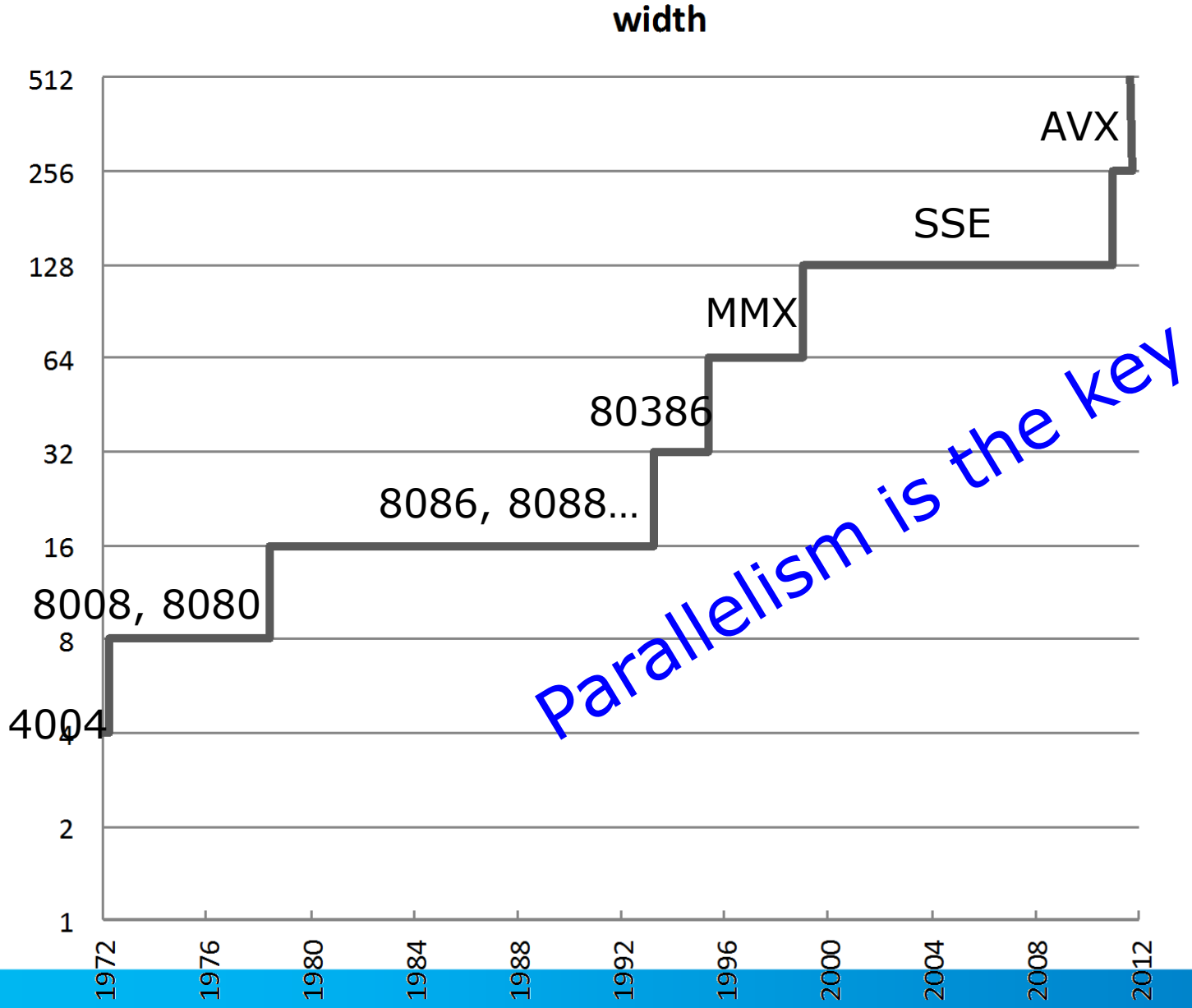
"Task parallelism"

Vectorization (wider vectors)

"Data parallelism"

Vector Growth

Parallel is the path forward



Two Types of Parallelism for Programmers to Identify and Use

Scaling (more cores)

"Task parallelism"

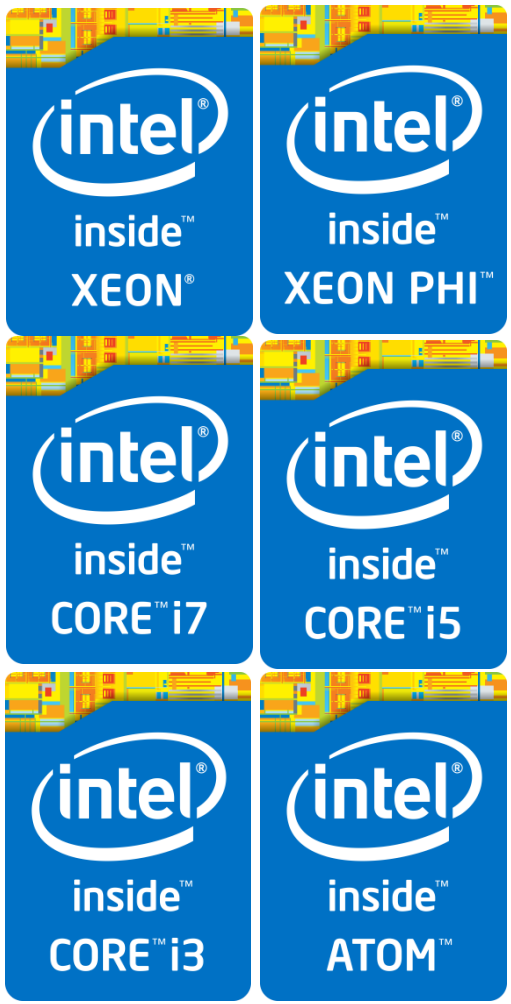
Vectorization (wider vectors)

"Data parallelism"

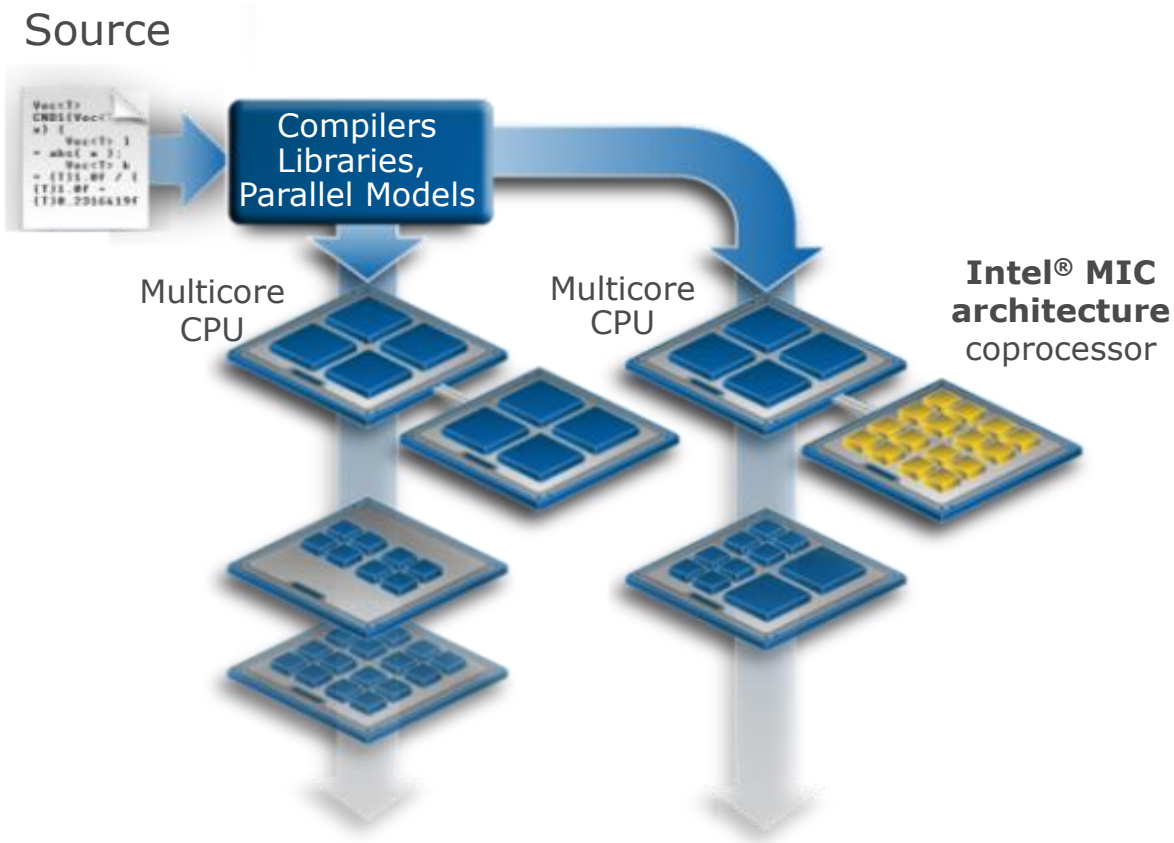
DATA LAYOUT / USAGE IS KEY

vision

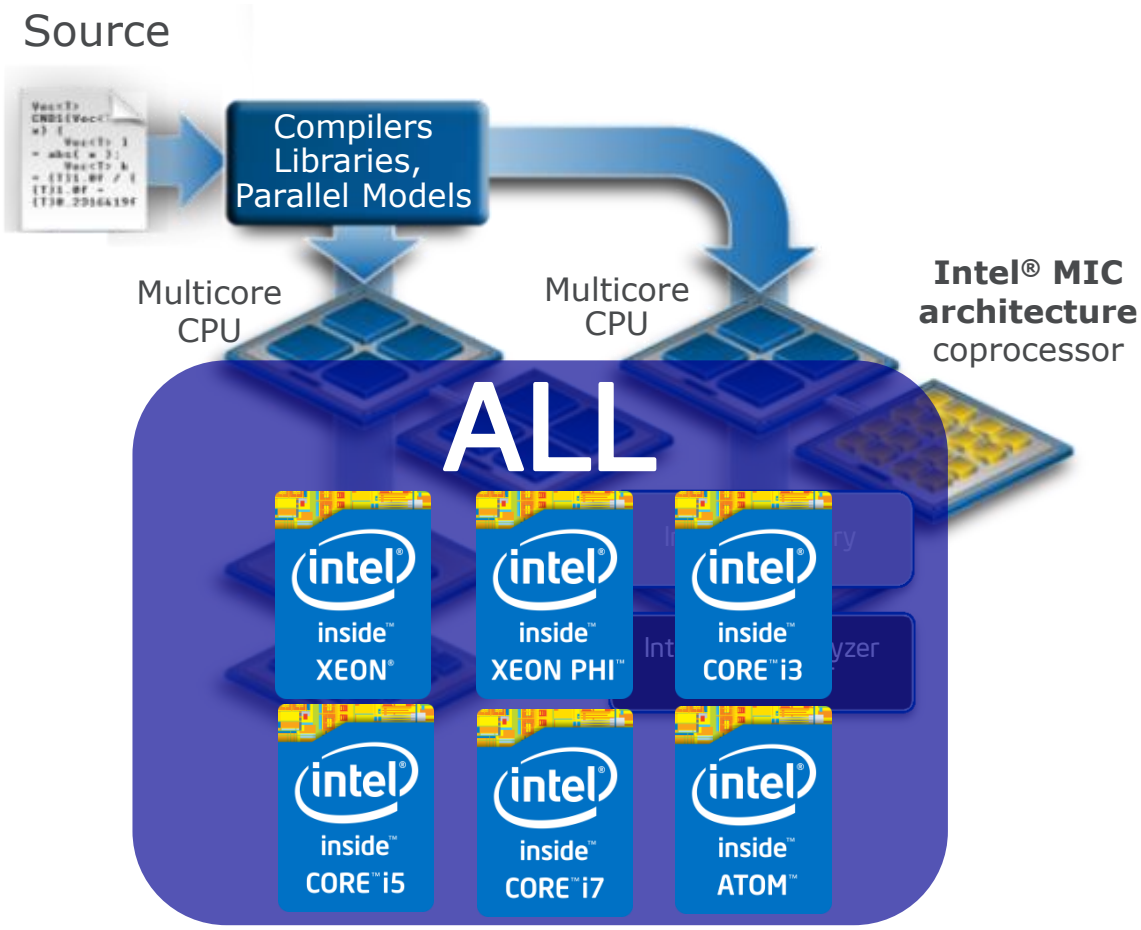
span from few cores to many cores with consistent models, languages, tools, and techniques



The Heterogeneous Architecture



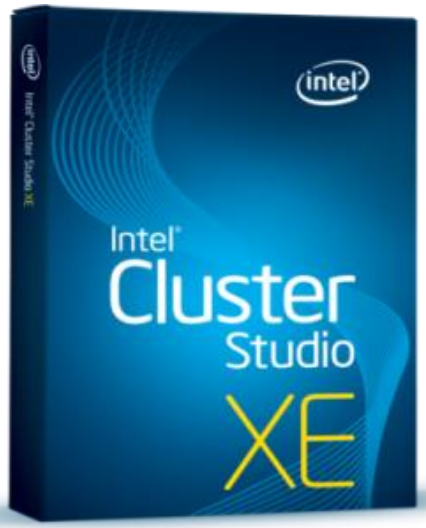
Neo-Heterogeneity – The Game Changer



"Unparalleled productivity… most of this software does not run on a GPU" - Robert Harrison, NICS, ORNL

R. Harrison, "Opportunities and Challenges Posed by Exascale Computing - ORNL's Plans and Perspectives", National Institute of Computational Sciences, Nov 2011"

Tools to Maximize Application Performance



Intel® C/C++ and Fortran Compilers w/OpenMP

Intel® MKL, Intel® Cilk Plus, Intel® TBB, and Intel® IPP

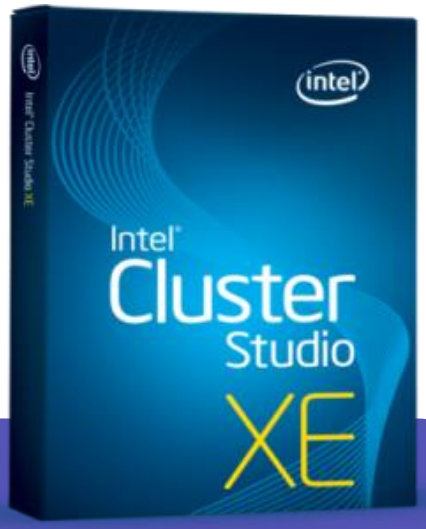
Intel® Inspector XE, **Intel® VTune™ Amplifier XE**, Intel® Advisor

+ Intel® MPI Library

+ Intel® Trace Analyzer and Collector

Intel® Parallel Studio XE

Unifying Intel® Architecture



ALL

Intel® C/C++ Compiler

Intel® MKL, Intel® TBB, IPP

Intel® VTune

Library

Analyzer

Parallel

XE

intel inside XEON

intel inside XEON PHI

intel inside CORE i3

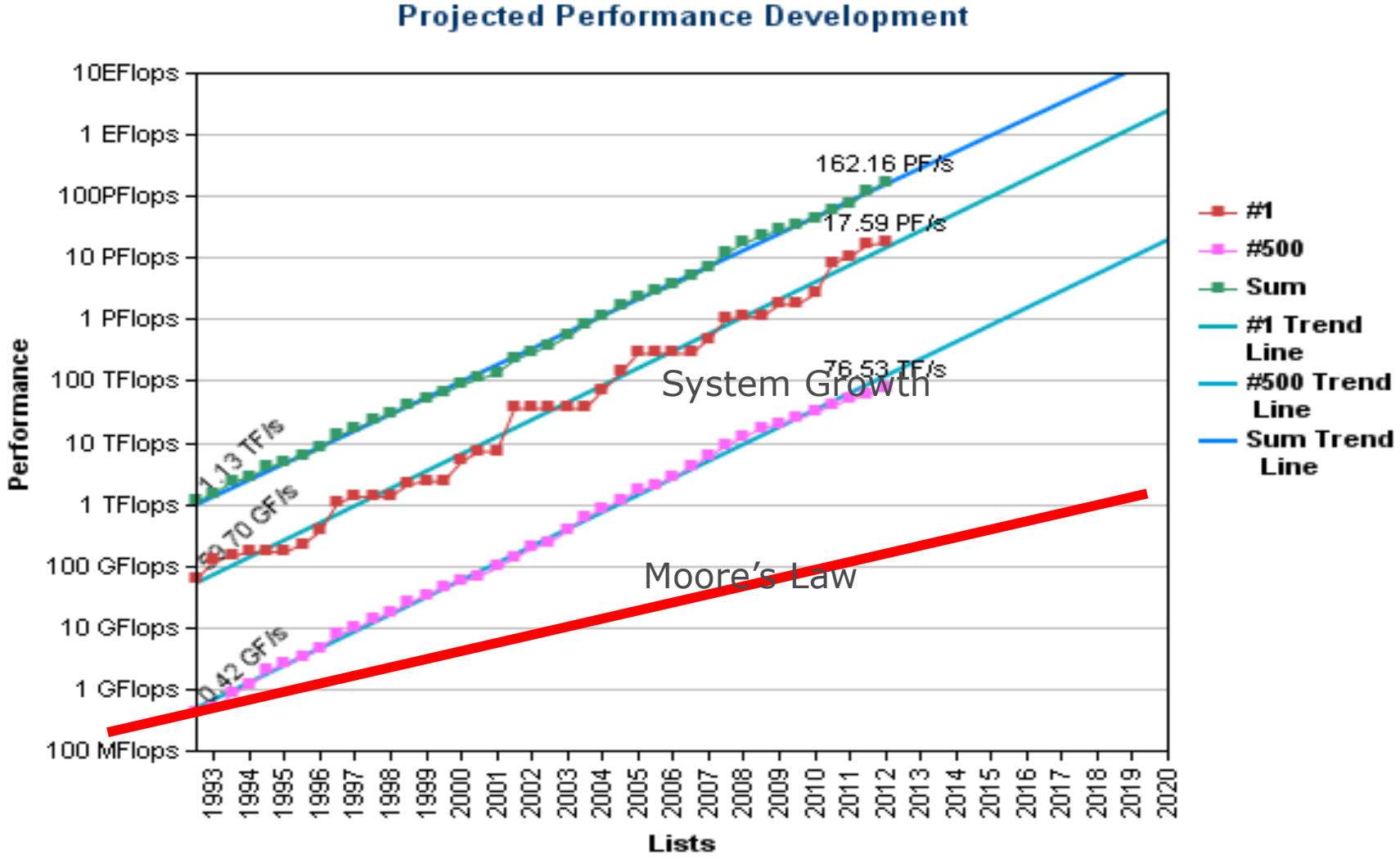
intel inside CORE i5

intel inside CORE i7

intel inside ATOM

Technical Trend #1: Top 500 System Performance—Faster than Moore's Law

Future requires heterogeneous computing & high performance fabric



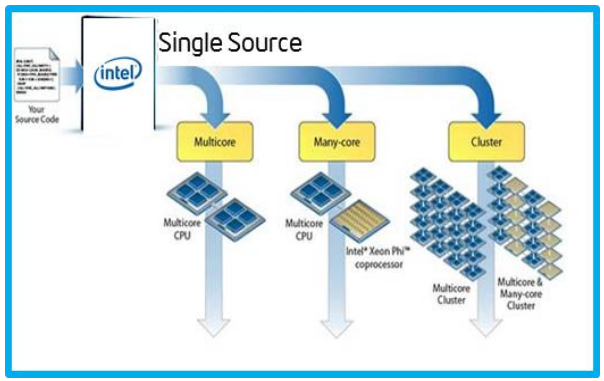
Neo-Heterogeneity at Scale

IDC HPC End-User MCS Study:
Overall Plans For Purchasing Coprocessors

IDC Analyze the Future

Q: What is your likely accelerator/co-processor purchase plans for your NEXT technical server purchase?

- 78.4% said YES – they plan to purchase coprocessors with their next HPC server
- This is more than double the 29.5% from our 2011 HPC End-User MCS study



IDC Intersect360

Heterogeneity is here to stay - 74% plan to buy…

…but it doesn't have to be HARD

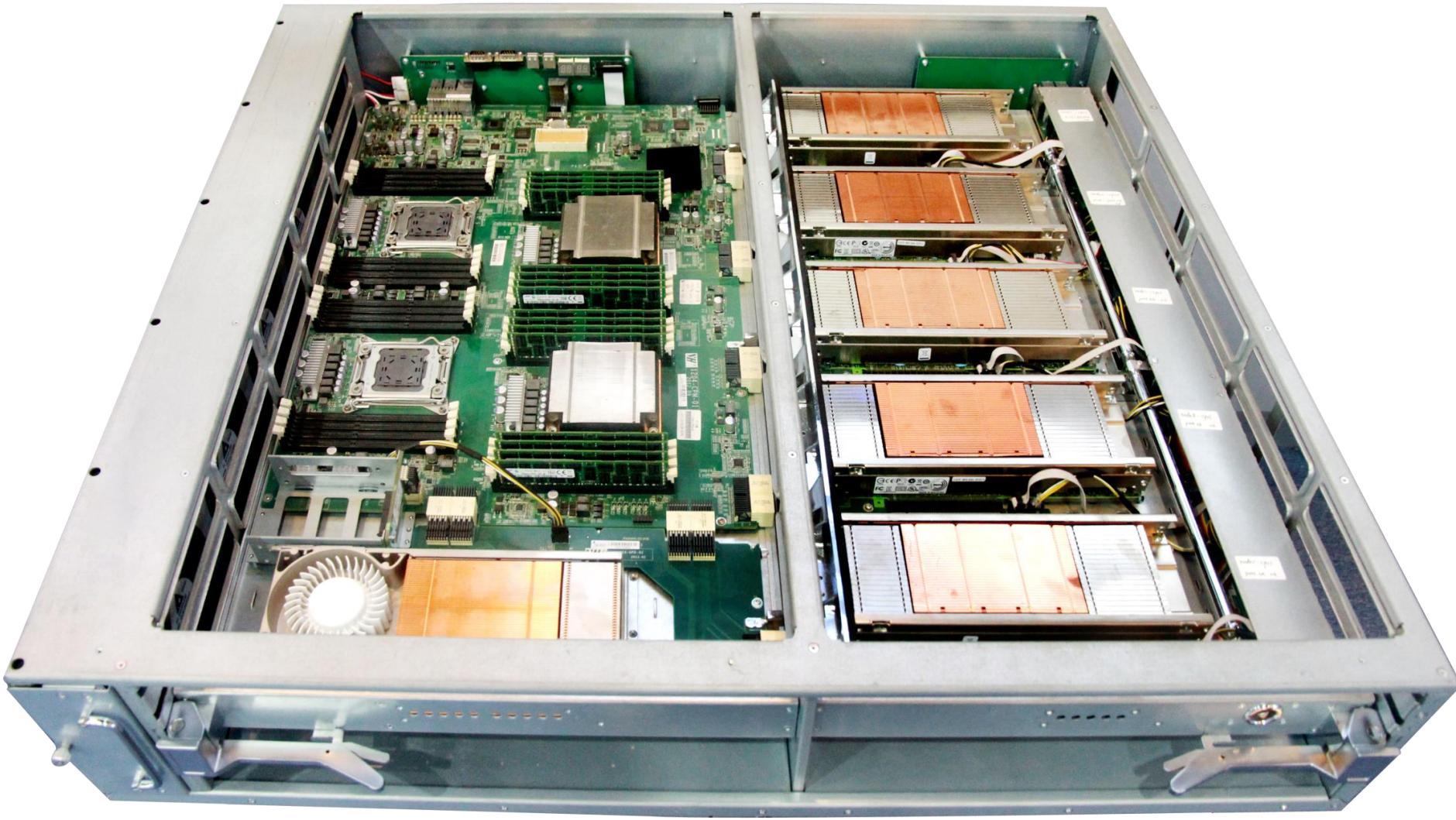
Neo- Heterogeneity = Heterogeneous system with a *single* programming model

Multiple Surveys: Increasing Intel Xeon Phi coprocessor user preference for future buys *and optimizing on Intel Xeon processor in general*

- Source: IDC. 78% surveyed plan to purchase a coprocessor or accelerator, Intersect360
- Source IDC: *Intel Xeon Phi leads all accelerators in user preference for future buys (Intel 32%, nVidia: 26%)*
- *IDC and Intersect360 names and brands may be claimed as the property of others.*

Milky Way 2 System – New Top500.org #1 System

What it looks like in action



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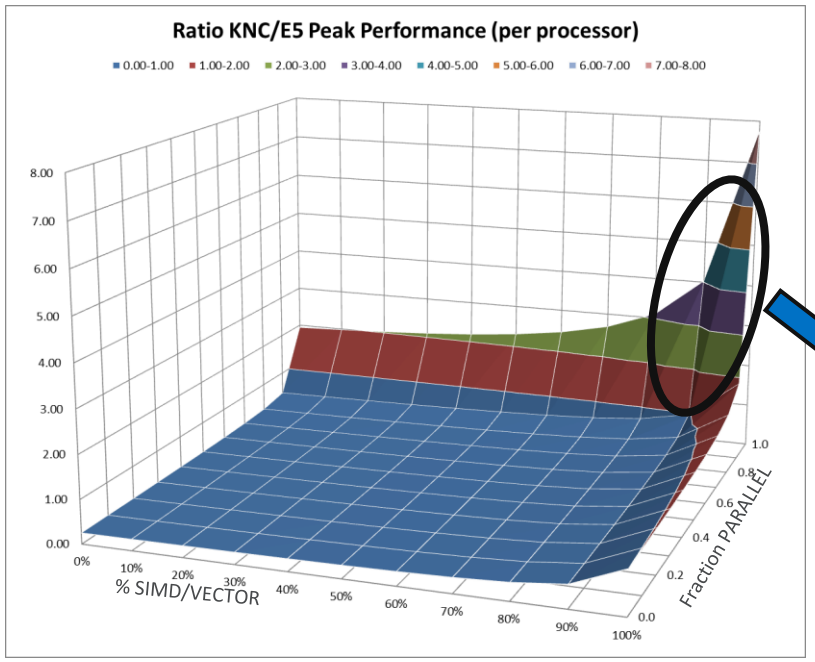
Intel® Xeon Phi™ Coprocessor:

Increases Application Performance up to 10x



KNC= Intel® Xeon Phi™ coprocessor (Knights Corner)
E5 = Intel® Xeon® E5 processor

Application Performance Examples

Customer	Application	Performance Increase[1] vs. 2S Xeon*
Los Alamos	Molecular Dynamics	Up to 2.52x
Acceleware	8th order isotropic variable velocity	Up to 2.05x
Jefferson Labs	Lattice QCD	Up to 2.27x
Financial Services	BlackScholes SP Monte Carlo SP	Up to 7x Up to 10.75x
Sinopec	Seismic Imaging	Up to 2.53x[2]
Sandia Labs	miniFE (Finite Element Solver)	Up to 2x[3]
Intel Labs	Ray Tracing (incoherent rays)	Up to 1.88x[4]

- Intel® Xeon Phi™ coprocessor accelerates highly parallel & vectorizable applications. (Chart)
- Table provides examples of such applications

Configuration Notes:

1. 2S Xeon vs. 1 Xeon Phi (preproduction HW/SW & Application running 100% on coprocessor unless otherwise noted)
2. 2S Xeon vs. 2S Xeon + 2 Xeon Phi (offload)
3. 8 node cluster, each node with 2S Xeon (comparison is cluster performance with and without 1 Xeon Phi per node) (Hetero)
4. Intel Measured Oct. 2012

DreamWorks Animation Workflow

Improved animation rendering time

Topline Innovation

Enables artists to preview and evaluate scenes more quickly as changes are made

Lighting modifications are viewed in near real-time instead of rendered overnight

Enables more immediate artist and production collaboration

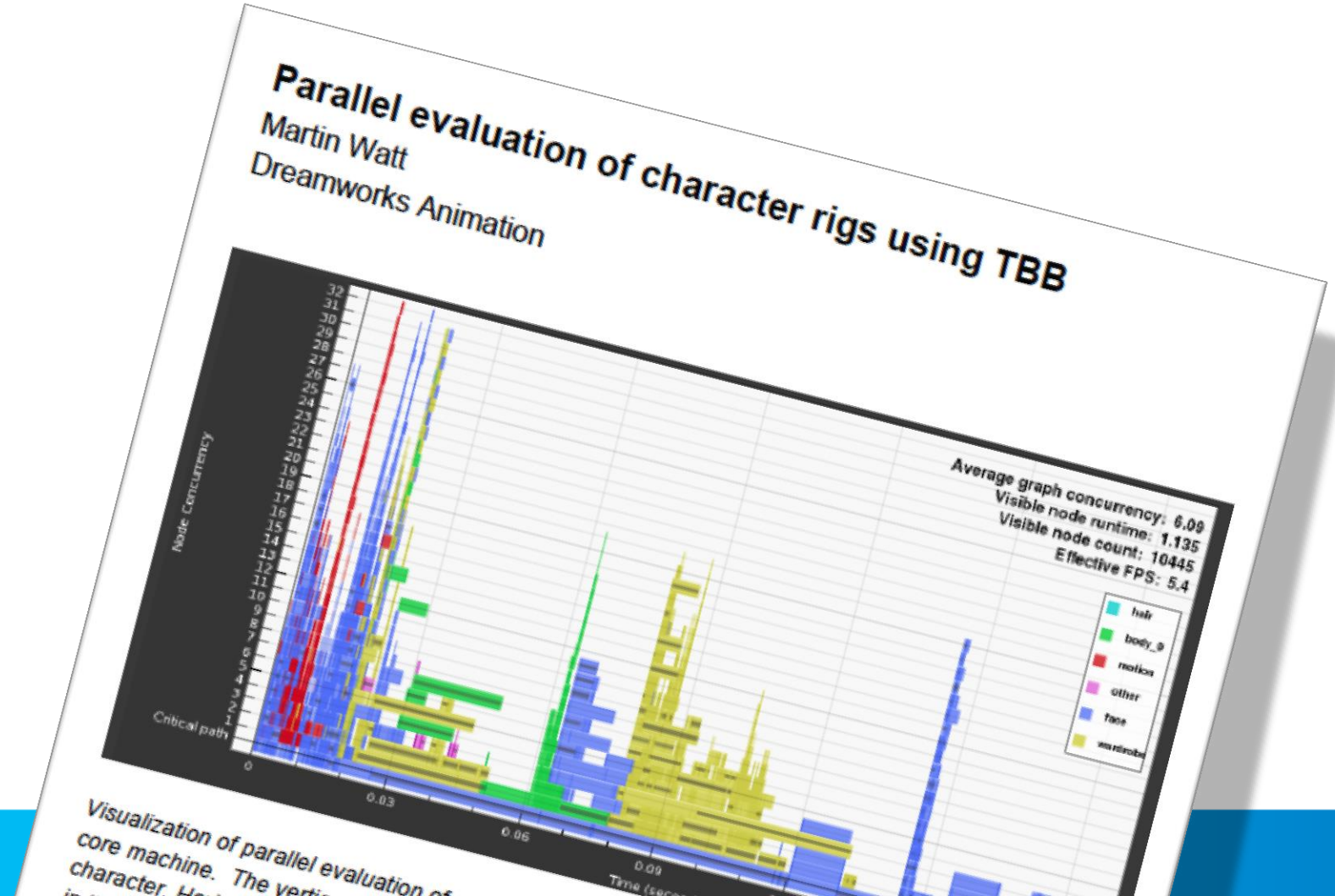
Bottom-line Benefits

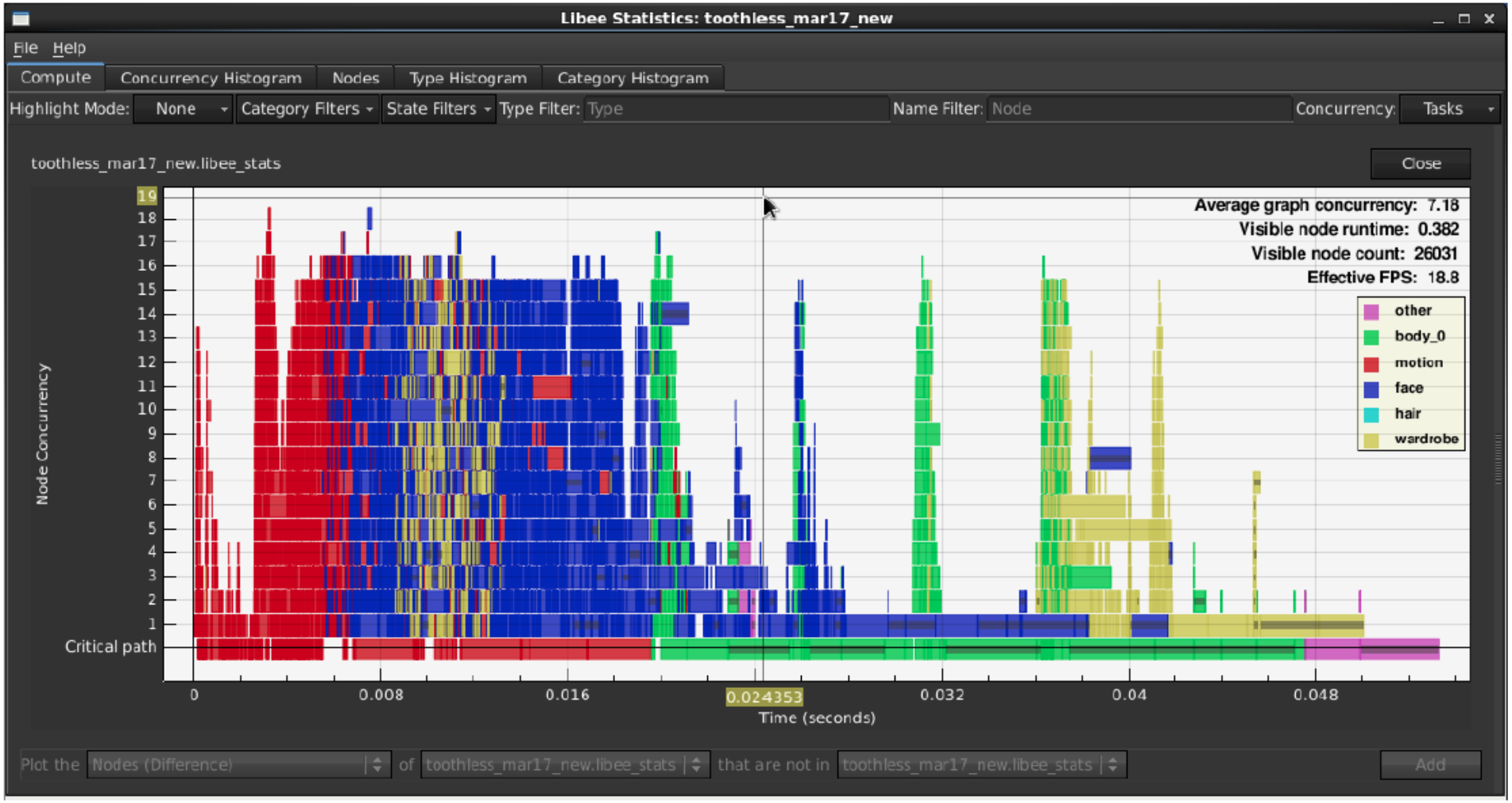
Reduces design environment complexity by improving workflow

Preserves software development investment while adopting new hardware technologies (i.e. Intel® Xeon Phi™ coprocessors)

Thread Visualization Tool @ Dreamworks
An example of the POWER of PARALLELISM

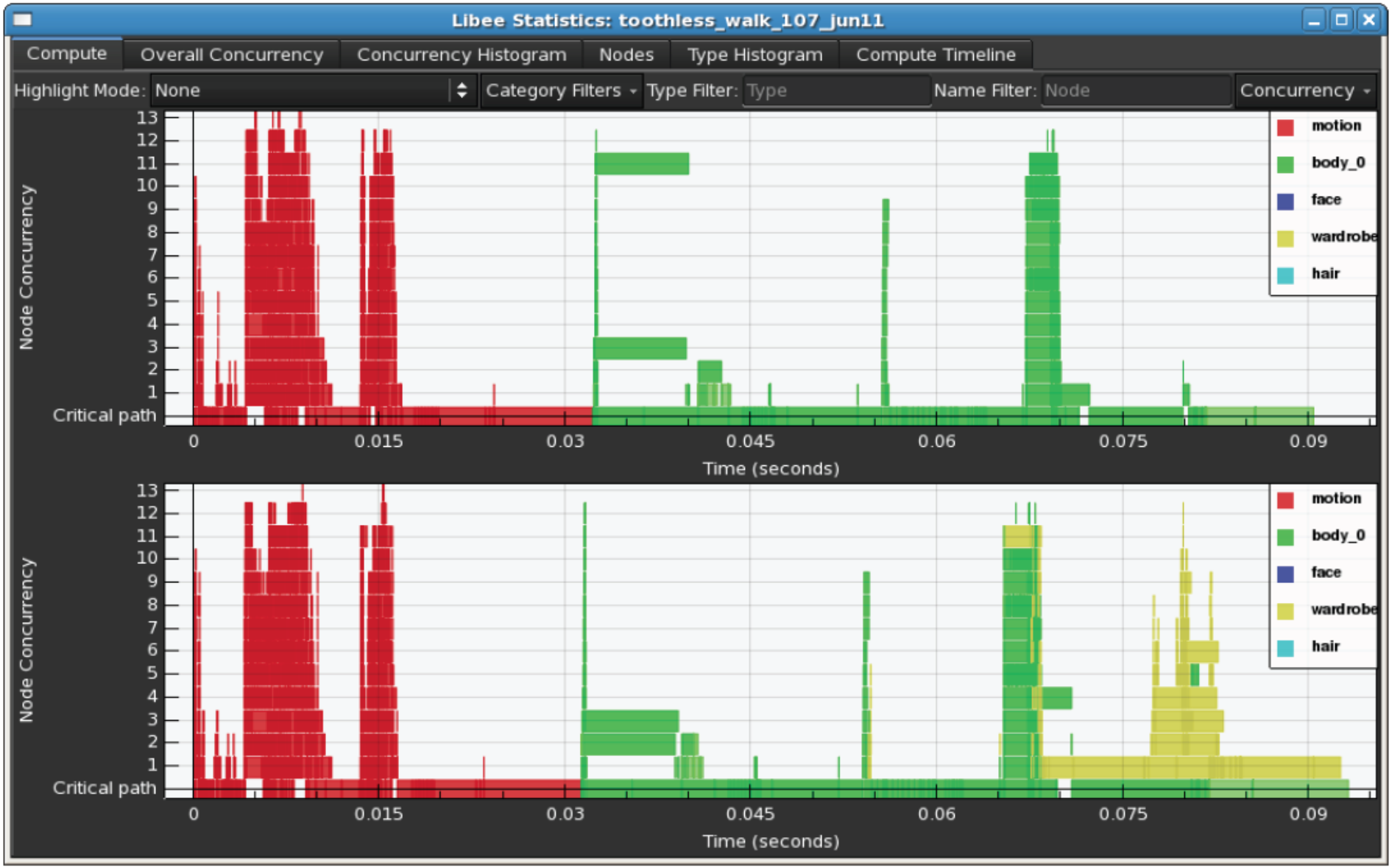
http://www.**multithreadingandvfx.org**/course_notes/





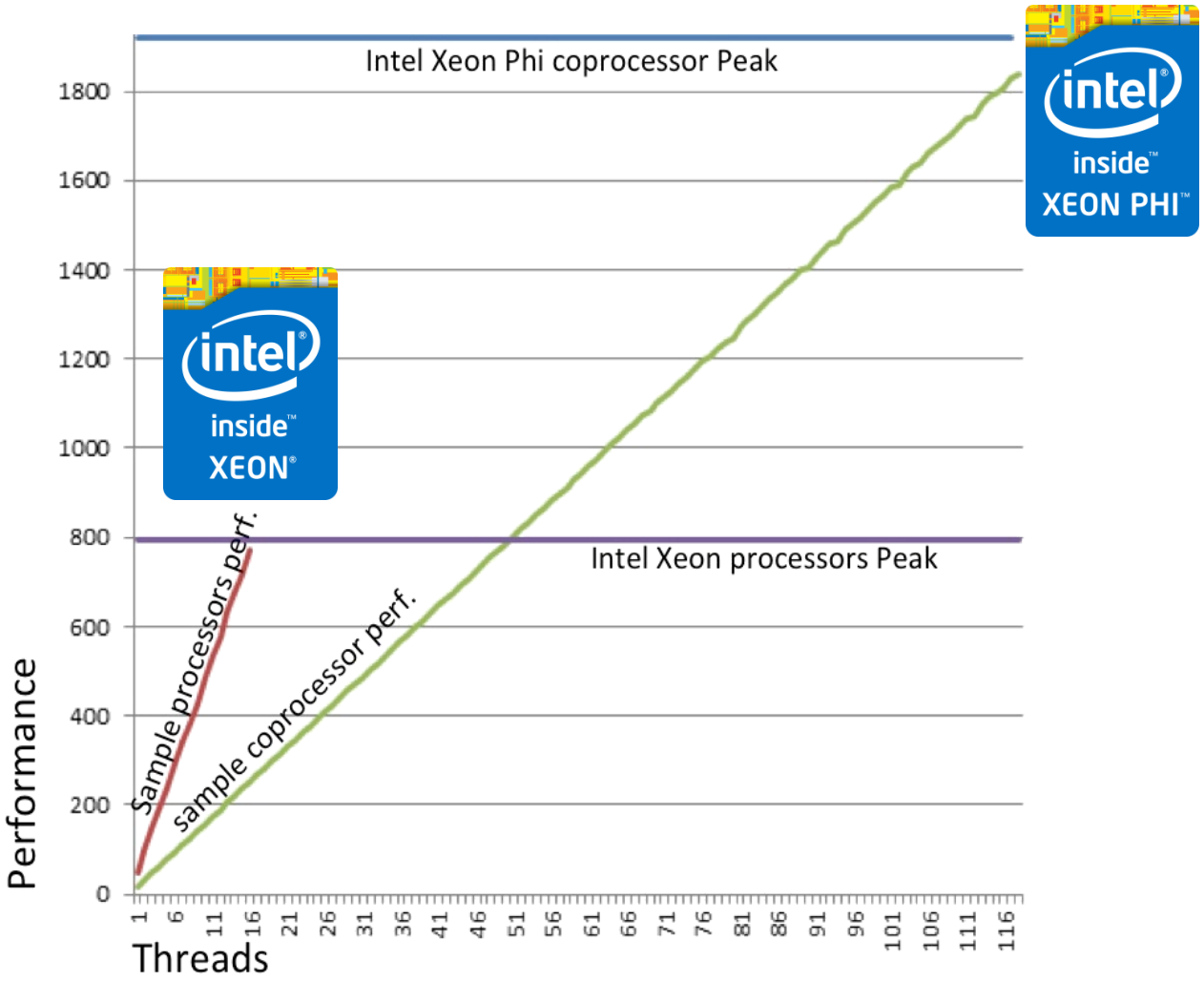
The threading visualization tool enables artists to investigate bottlenecks within the graph. The tool highlights different character rig components in different colors (i.e. body, face, wardrobe, and hair) and provides overall graph concurrency statistics. Note that the average concurrency only represents graph parallelism and does not include node parallelism. The bottom row of nodes are the nodes on the critical path.

Mode to compare two profiles to check benefits of optimizations



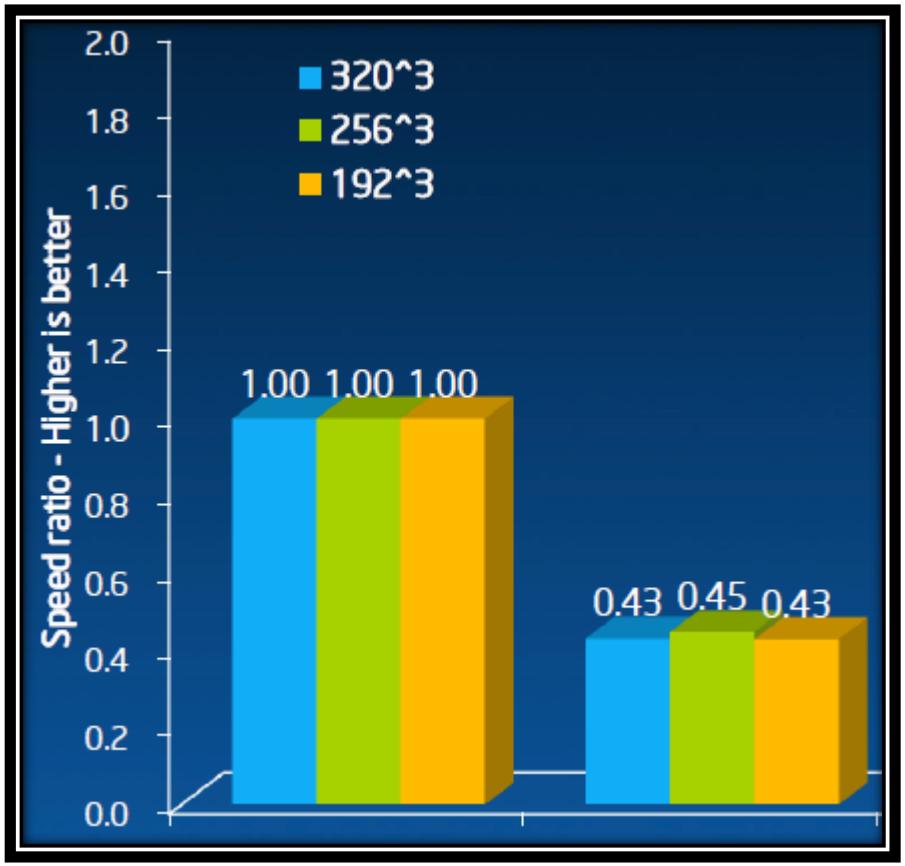
Top graph shows character with motion and deformation system, bottom graph shows addition of clothing. Note that the overall runtime increases only marginally although there is significant extra work being performed in the rig.

Picture worth many words



Illustrative example

Fortran code using MPI, single threaded originally.
Run on Intel® Xeon Phi™ coprocessor natively (no offload).



Based on an actual (but confidential) customer example. Shown to illustrate a point about common techniques. Your results may vary!

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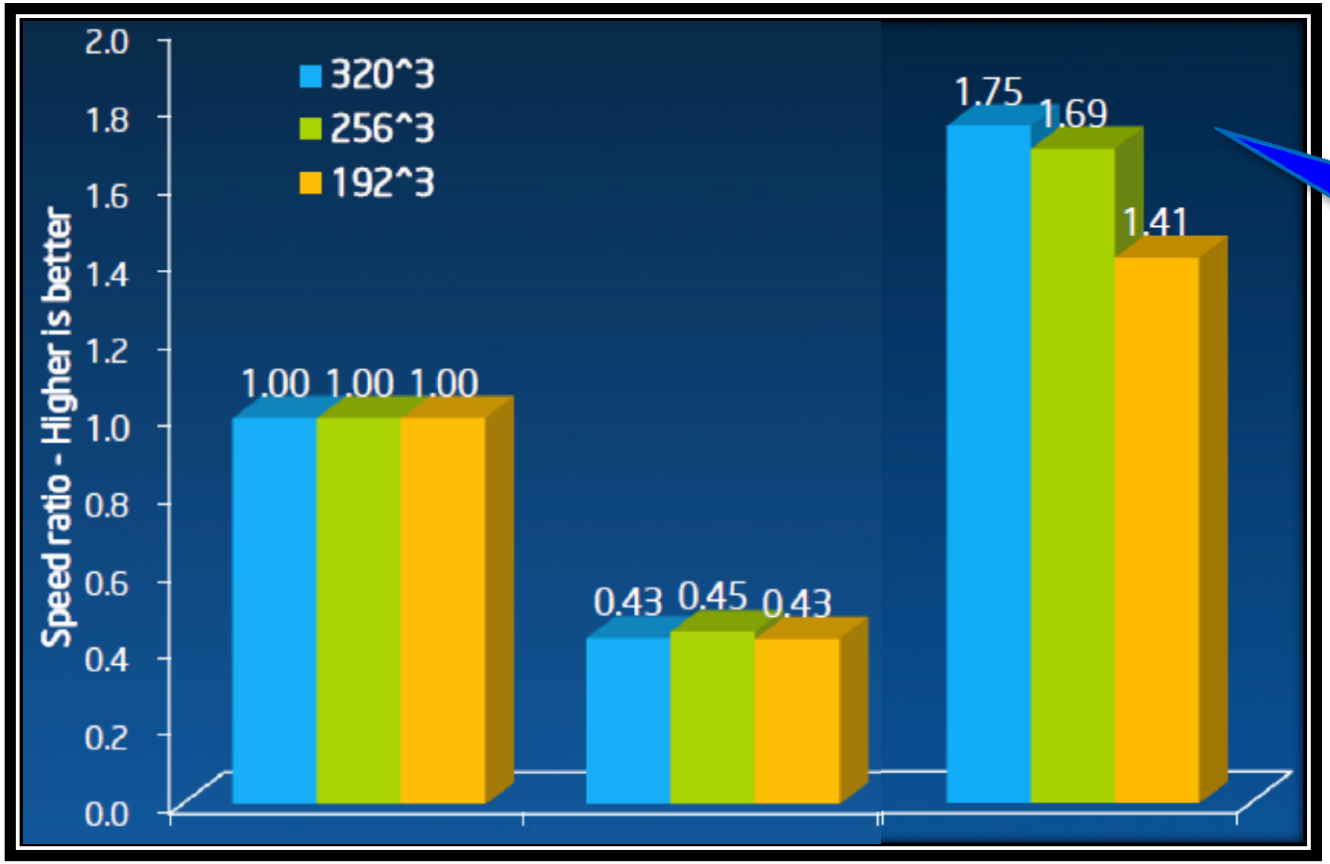

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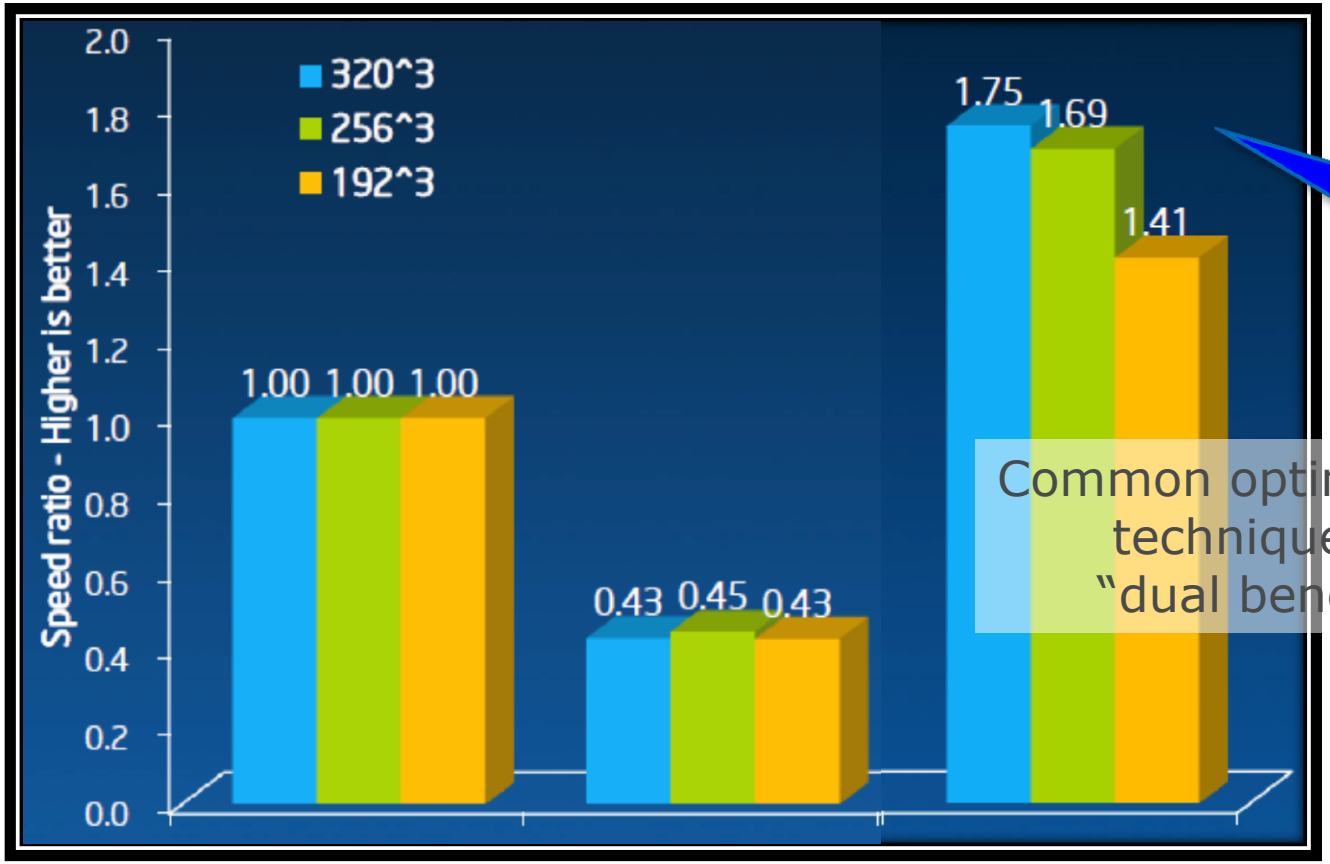

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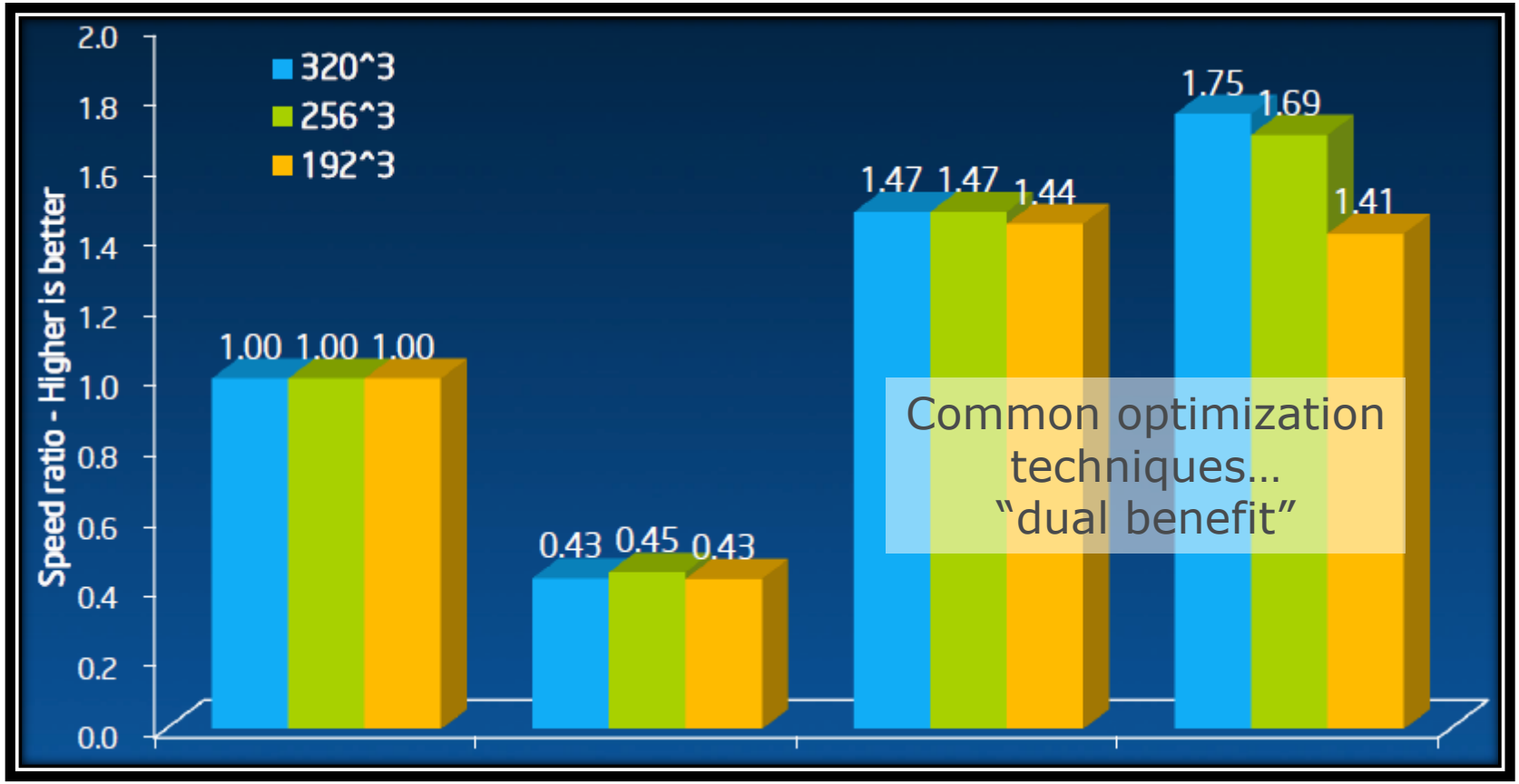

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Intel® Parallel Studio XE 2013 SP1 & Intel® Cluster Studio XE 2013 SP1

Faster code + Simplified development

$1,599-$2,299

$2,949

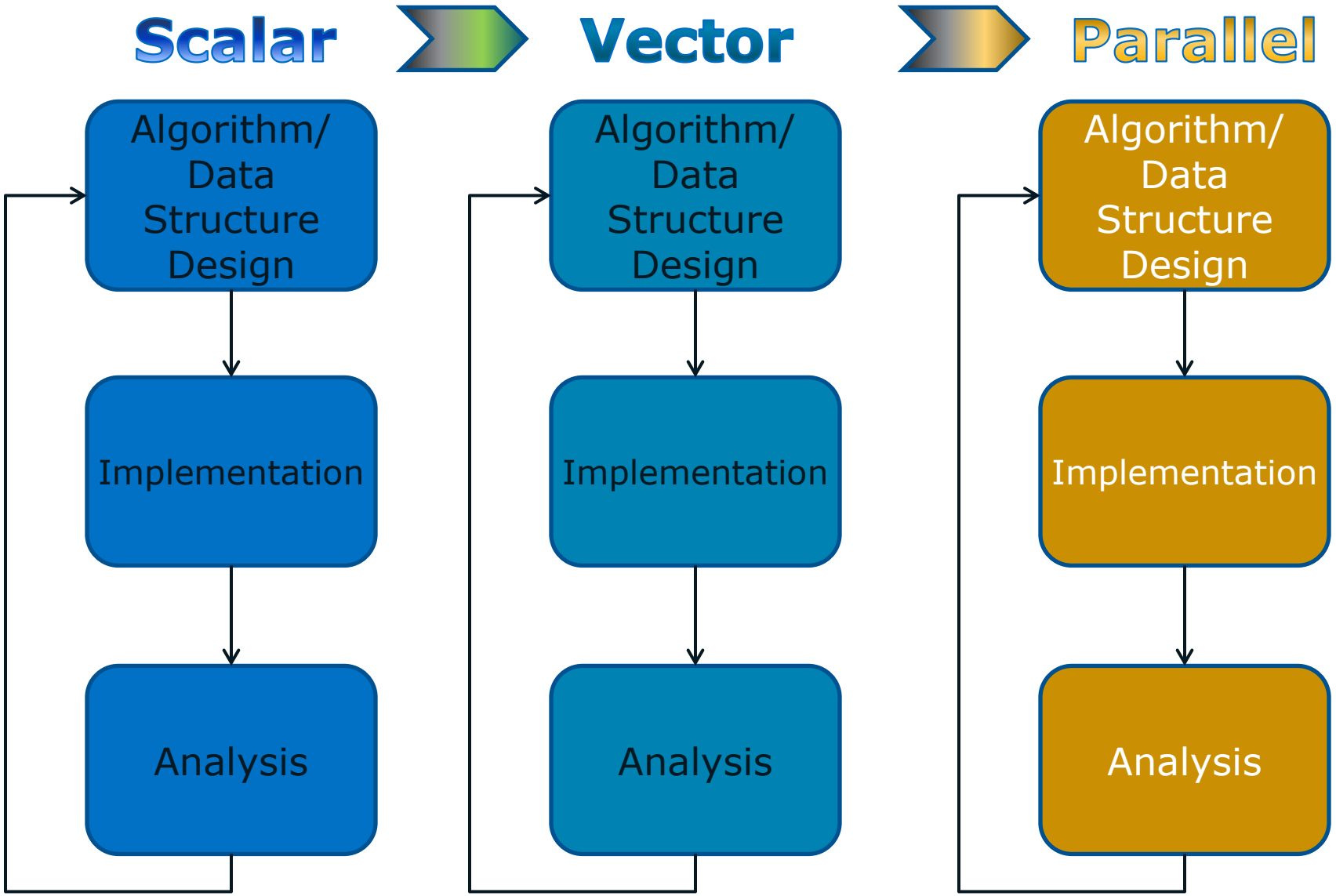
"SP1" release shipping since September 4, 2013

Top New Features

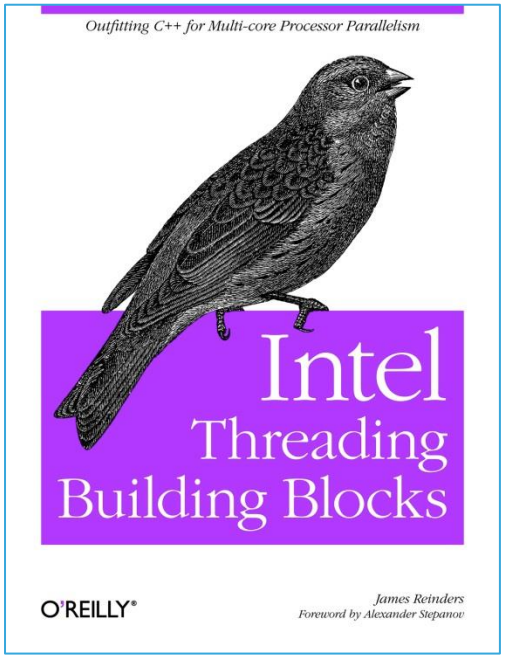
Performance	Analysis Efficiency	Productivity	Cross Platform Portability
Improved compiler and library performance	Better data mining for performance tuning	Improved conditional numerical reproducibility	OpenMP* 4.0 SIMD and target constructs
Intel® AVX-512 ready	Simplified scalability testing for OpenMP*	Enhanced GDB for Linux* and OS X*	Expanded C++11
Broadwell & Haswell-EP microarchitecture optimizations	Incremental analysis and easier suppression management		Expanded Fortran 2003 & 2008
Windows* support for Intel® Xeon Phi™ coprocessor	Enhanced MPI analysis interface		Improved MPI Performance and Scalability

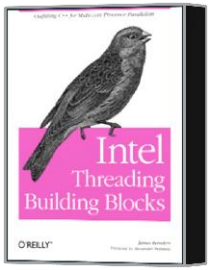
More info at: http://intel.ly/perf-tools

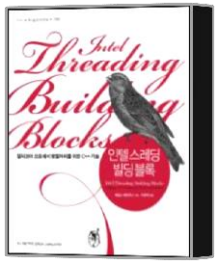
Optimization Framework



www.threadingbuildingblocks.org







- ✓ **Most popular C++ abstraction**
- ✓ **Windows***
- ✓ **Linux***
- ✓ **OS* X**
- ✓ **Xbox 360**
- ✓ **Solaris***
- ✓ **FreeBSD***
- ✓ **Intel processors**
- ✓ **AMD processors**
- ✓ **SPARC processors**
- ✓ **IBM processors**
- ✓ **open source**
- ✓ **standard committee submissions**

The most used method to parallelize C++ programs

It all comes down to PARALLEL PROGRAMMING ! (applicable to processors and Intel® Xeon Phi™ coprocessors both)

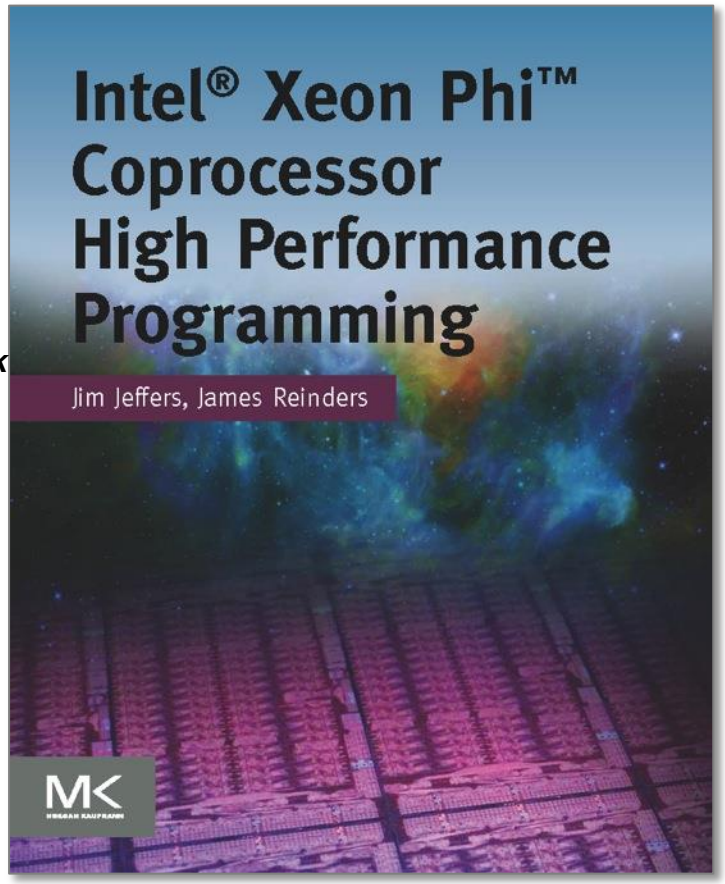
Forward, Preface
Chapters:

1. *Introduction*
2. *High Performance Closed Track Test Drive!*
3. *A Friendly Country Road Race*
4. *Driving Around Town: Optimizing A Real-World Code Example*
5. *Lots of Data (Vectors)*
6. *Lots of Tasks (not Threads)*
7. *Offload*
8. *Coprocessor Architecture*
9. *Coprocessor System Software*
10. *Linux on the Coprocessor*
11. *Math Library*
12. *MPI*
13. *Profiling and Timing*
14. *Summary*

Glossary, Index

Learn more about this book:

lotsofcores.com



Available since February 2013.

This book belongs on the bookshelf of every HPC professional. Not only does it successfully and accessibly teach us how to use and obtain high performance on the Intel MIC architecture, it is about much more than that. It takes us back to the universal fundamentals of high-performance computing including how to think and reason about the performance of algorithms mapped to modern architectures, and it puts into your hands powerful tools that will be useful for years to come.
—Robert J. Harrison
Institute for Advanced Computational Science, Stony Brook University

Intel® Xeon Phi™ Coprocessor High Performance Programming, Jim Jeffers, James Reinders, (c) 2013, publisher: Morgan Kaufmann

Teaches parallel programming using a new pattern-based approach.

Extensive examples in Cilk Plus and TBB.

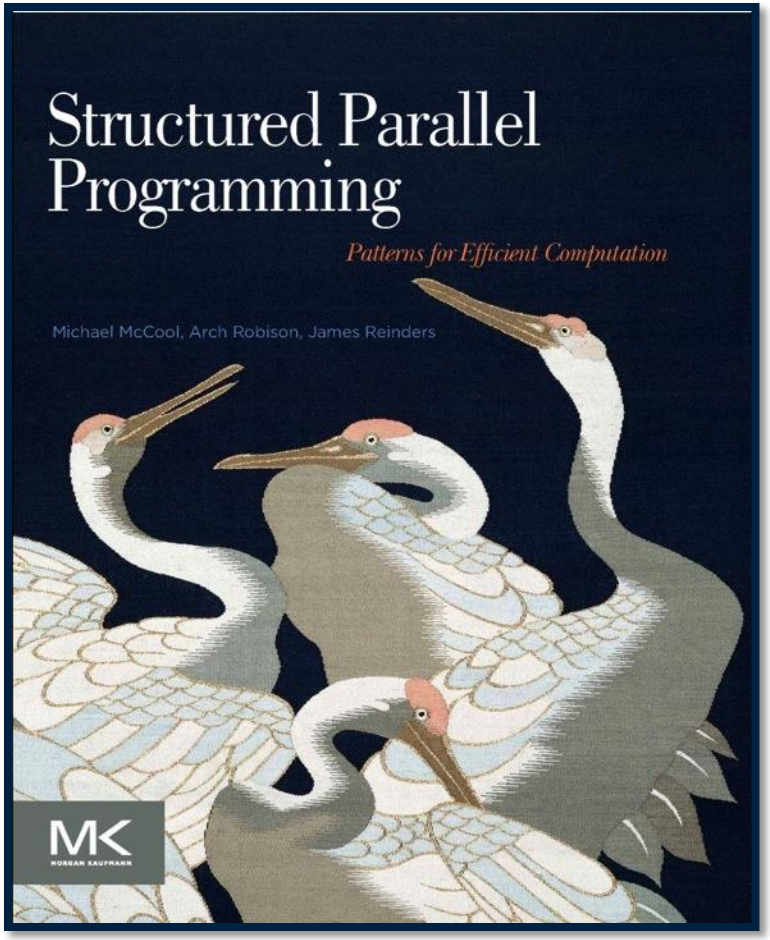
Not about any specific hardware, but relevant to all.

It's about effective parallel programming.

Great for teaching!

Learn more about this book:

parallelbook.com



Available since July 2012.

SC'13 tutorial
November 2013
In Denver

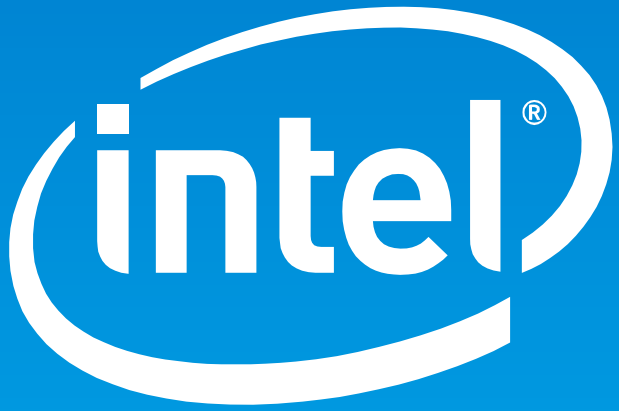
This is a really great book…

I've been dreaming for a while of a modern accessible book that I could recommend to my threading-deprived colleagues and assorted enquirers to get them up to speed with the core concepts of multithreading as well as something that covers all the major current interesting implementations.

Finally I have that book.

—Martin Watt, Principal Engineer, Dreamworks Animation

Structured Parallel Programming, Michael McCool, Arch Robison, James Reinders
(c) 2012, publisher: Morgan Kaufmann


intel

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Simulated Results Benchmark Disclaimer: Results have been simulated and are provided for informational purposes only. Results were derived using simulations run on an architecture simulator or model. Any difference in system hardware or software design or configuration may affect actual performance.

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Rev. 7/17/13